Systematic Design of Analog CMOS Circuits Using Lookup Tables

We show in this tutorial how a Circuit Simulator like SPICE can be put to use in order to assess systematically currents and sizes of MOS transistors. Generally, sizing is done running SPICE while adjusting parameters until we achieve prescribed performances. While this iterative procedure leads to the assessment of correct parameters, it does not allow us to take advantage of analytic expressions concomitantly. This prevents us from the possibility to optimize sizes and currents in the same time.

The objective of this tutorial is to present a sizing methodology that allows us to make use of analytical expressions while taking advantage of (exact) bias dependent parameters in the same time. The so-called (exact) parameters are extracted from precomputed lookup tables previously derived from a circuit simulator, like SPICE. Features like gain, current consumption, … not only are evaluated correctly this way but they can be optimized without the need to run repeated simulations too.

The key ideas behind the sizing methodology can be summarized as follows:

1) Use ratios of parameters that are assumed to vary like the width of transistors, e.g. g_m, g_{ds}, C_{gg} …. Most analog CMOS circuits, especially high frequency and subthreshold circuits, comply with this assumption.
2) Extract the magnitudes of parameter ratios from precomputed lookup tables. These need to be evaluated only once for any given circuit simulator.

To take a simple example, consider a common source MOS transistor loaded by a capacitor. The transistor is fed by an ideal current source. Assume we want to achieve a prescribed GBW product, which implies that the transconductance g_m is fixed a priori. We choose the transconductance efficiency (g_m/I_D) as the prime parameter. This fixes automatically the magnitude of the drain current I_D. To evaluate the width of the transistor, all we need is to extract the drain current density (I_D/W) from J_D lookup tables. To enter these, we specify the drain to source voltage V_{DS} and the gate length L, unless the transit frequency (g_m/C_{gg}) being given, the gate length is known.

More complex circuits, like a high impedance large swing current mirror, an LDO, …are considered. The outcome of every sizing procedure is checked against straightforward SPICE verifications.

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