Title: Fault Tolerant Techniques for Integrated Circuits

Abstract: Integrated circuits fabricated in CMOS or Finfet are susceptible to radiation-induced faults at space and at ground level. A large variety of techniques to mitigate these faults can be applied from process technology, transistor arrangements, logic and system-level redundancy. The key is to select the most appropriate technique or set of techniques that can meet the design constraints. This tutorial will present some of the state-of-the-art techniques and some case studies implementations.

Speaker: Prof. Fernanda Lima Kastensmidt

Bio: Fernanda Kastensmidt holds a degree in Electrical Engineering from the Federal University of Rio Grande do Sul (1997), a master's degree in Computer Science from the Federal University of Rio Grande do Sul (1999) and a doctorate in Computer Science from the Federal University of Rio Grande do Sul (2003). She is currently Associate Professor at the Federal University of Rio Grande do Sul and Coordinator of the Graduate Program in Microelectronics (PGMICRO). She has experience in Microelectronics and Computer Engineering, focusing on Hardware, acting on the following subjects: radiation fault protection techniques, fault tolerant systems design, programmable architecture, FPGA, systems qualification and fault integrated circuits and fault modeling. She is the author of the book Fault Tolerance Techniques for SRAM-based FPGAs published in 2006 by Springer and co-author of 3 more scientific books. Participated in the NanoSat-BR1 satellite payload project which was launched in June 2014 and is currently in the NanoSat-BR2 project where part of the payload is responsible for analyzing the effects of SAA on Integrated Circuits manufactured using nanometer technology. Besides on being a professor at UFRGS, Fernanda is registered as a researcher at CNPq (Researcher Agency in Brazil), classified as researcher level 1.